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Docket No.: 218433US2

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COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 10/057,952
Applicants: Akio NAKAYAMA et al.
Filing Date: January 29, 2002
For: LIQUID CRYSTAL DISPLAY DEVICE AND MANUFACTURING METHOD THEREFOR
Group Art Unit: 2871
Examiner: DI GRAZIO, J. A.

SIR:

Attached hereto for filing are the following papers:

APPEAL BRIEF with APPENDICES

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Respectfully submitted,

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:	
AKIO NAKAYAMA ET AL.	:	EXAMINER: DI GRAZIO, J. A.
SERIAL NO: 10/057,952	:	
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APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an Appeal Brief of the Final Office Action dated March 23, 2005, of Claims 1-3, 8, 9, 11, 12, 16, and 17. A Notice of Appeal from this Final Office Action was timely filed on July 25, 2005.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee Significant Display Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants, appellants' legal representatives, and the assignee are not aware of any other appeals, interferences, or judicial proceedings that would directly effect or be directly affected or having a bearing on the Board's decision in the pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-3, 8, 9, 11, 12, 16, and 17 stand finally rejected. Claims 4-7, 14-15, and 18 were withdrawn from consideration and Claims 10 and 13 have been canceled without prejudice during prosecution. Claims 1-3, 8, 9, 11, 12, 16, and 17 are on appeal. A clean copy of the pending Claims 1-9, 11, 12, and 14-18 is attached in the Claims Appendix.

IV. STATUS OF THE AMENDMENTS

No amendment was filed after the Notice of Appeal or after the Final Office Action of March 23, 2005. However, a Request for Reconsideration was filed on June 22, 2005, after the Final Office Action, but the Advisory Action of July 11, 2005, indicated that Claims 1-9, 11, 12, and 14-18 stand rejected.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 is directed to a liquid crystal display device that includes transistors disposed at the intersections of gate lines and source lines as shown for example in Figures 1 and 2. For example, Figure 1 shows a gate line 2 and a source line 7 and a transistor (4, 8, and 9) formed at the intersection of the gate line 2 and the source line 7 (see the original specification at page 16, first full paragraph). The liquid crystal display device includes pixel electrodes connected to the transistors (see pixel electrodes 14 and 16 in Figures 1 and 2). Opposite to the pixel electrodes are opposite electrodes 24 as disclosed in the specification at page 17, first full paragraph. A liquid crystal 26 is held between the

opposite electrodes and the pixel electrodes as shown in Figure 3 and disclosed in the specification at page 17, first full paragraph. The pixel electrodes include a first pixel electrode 16 and a second pixel electrode 14 as shown in Figures 1-3 (see the original specification at page 17, lines 4-7). The second pixel electrode 14 is disposed in a layer above an insulating film 101 as disclosed in the specification at page 17, lines 7-9, and shown in Figure 3. The insulating film 101 is disposed above the first pixel electrode 16 and the second pixel electrode 16 has a region that does not overlap with the first pixel electrode 14, as disclosed in the specification at page 17, lines 9-11. The first pixel electrode 16 and the second pixel electrode 14 are electrically connected as shown in Figure 3 and disclosed in the specification at page 17, lines 11-13. The first pixel electrode applies a first electric field to the liquid crystal and the second pixel electrode applies a second electric field having a strength different from the first electric field to the liquid crystal, as disclosed in the specification in the paragraph bridging pages 29 and 30. A ratio of a first voltage applied to the liquid crystal by the first pixel electrode and a second voltage applied to the liquid crystal by the second pixel electrode is 0.5:1.0 to 0.9:1.0, as disclosed in the specification in the paragraph bridging pages 30 and 31.

Independent Claim 9 recites similar features as independent Claim 1 except that Claim 9 recites that the first pixel electrode and the second pixel electrode are electrically connected to a drain electrode 9 as shown in Figures 1 and 2 and disclosed in the specification at page 16, first full paragraph.

Independent Claim 16 is directed to a method for manufacturing a liquid crystal display device having transistors disposed at the intersections of gate lines and source lines, pixel electrodes connected with the transistors, opposite electrodes opposite to the pixel electrodes, and a liquid crystal held between the opposite electrodes and the pixel electrodes as discussed above regarding independent Claims 1 and 9.

The method includes a step of manufacturing a first pixel electrode that applies a first electric field to the liquid crystal as disclosed in the specification at page 17, lines 18-20. A step for manufacturing an insulating layer in a layer above the first pixel electrode is disclosed in the specification at page 18, lines 6-8, and a step for manufacturing a second pixel electrode in a layer further above the insulating layer is disclosed in the specification at page 18, lines 9-10.

As discussed above regarding independent Claim 1, the second pixel electrode has a region that does not overlap the first pixel electrode, as shown for example in Figure 2. The second pixel electrode 14 is electrically connected to the first pixel electrode 16 and applies a second electric field having a strength different from the first electric field applied to the liquid crystal. As discussed in the originally filed specification in the paragraph bridging pages 30 and 31, a ratio of the voltages applied to the liquid crystal by the first pixel electrode and the second pixel electrode is 0.5:1.0 to 0.9:1.0.

Independent Claim 17 recites features similar to independent Claim 16 except that Claim 17 recites that the second pixel electrode 14 shown in Figure 2 is connected to the drain electrode 9.

VI. GROUNDS OF REJECTIONS TO BE REVIEWED ON APPEAL

Appellants respectfully request the Board to review on this Appeal: (i) the rejection of Claims 1, 9, 11, 12, 16, and 17 under 35 U.S.C. § 103(a) as unpatentable over Michibayashi et al. (U.S. Patent No. 5,680,190, herein "Michibayashi") in view of Kaneko et al. (U.S. Patent No. 5,777,700, herein "Kaneko"); (ii) the rejection of Claims 2 and 3 under 35 U.S.C. § 103(a) as unpatentable over Michibayashi in view of Kaneko and Kim et al. (U.S. Patent No. 6,198,516 B1, herein "Kim"); and (iii) the rejection of Claim 8 under 35 U.S.C. § 103(a)

as unpatentable over Michibayashi, Kaneko, and Lee et al. (U.S. Patent No. 6,215,542 B1, herein "Lee").

VII. ARGUMENT

A. The combination of Michibayashi and Kaneko is improper and does not teach or suggest each of the features of independent Claims 1, 9, 16, and 17.

Independent Claim 1 subject matter has been discussed above.

Turning to the applied art, Michibayashi discloses a liquid crystal display apparatus having a transistor 25 disposed at the intersection of a gate line and a source line (not labeled) as shown in Figure 1B. Michibayashi shows in Figure 1A that pixel electrodes 23a and 23b are disposed such that only one of the pixel electrodes, 23a, is electrically connected to the transistor 25 and the other pixel electrode 23b is not electrically connected to the transistor 25, which is different from the claimed device. In other words, the pixel electrodes of Michibayashi are capacitively coupled while the claimed pixel electrodes "are electrically connected."

To overcome this deficiency, the Final Office Action relies on another embodiment of Michibayashi shown in Figure 9. Figure 9 shows a first pixel electrode 42an and a second pixel electrode 42bm that are electrically connected to each other. However, Michibayashi does not teach or suggest that the first and second electrodes 42an and 42bm shown in Figure 9 are connected to the transistor 13 of Figure 9. In addition, the Final Office Action does not provide any motivation for combining the device shown by Michibayashi in Figure 9 with the device shown in Figure 1A to arrive at the claimed subject matter. Thus, at least for this reason, the combination of Michibayashi and Kaneko is improper.

Further, the Final Office Action recognizes at page 4, first full paragraph, that "Michibayashi does not appear to explicitly specify that a ratio of a first voltage applied to

the liquid crystal by the first pixel electrode and a second voltage applied *to the liquid crystal* by the second pixel electrode is 0.5:1.0 to 0.9:1.0" (original emphasis). The Final Office Action relies on the Appellants' specification and Kaneko for teaching the features lacking in Michibayashi.

Appellants note that Kaneko does not explicitly disclose the above-noted feature that lacks in Michibayashi. In fact, the Final Office Action, relying on the disclosure of the Appellants (see Final Office Action, paragraph bridging pages 4 and 5), suggests that Kaneko, by teaching a thickness of an insulation film equal to the thickness of the insulation film disclosed in the specification, will achieve the claimed ratio of the first and second voltages.

More specifically, the Final Office Action relies on the description at page 30, lines 7-10 of the Appellants' specification, to assert that the claimed ratio of the first voltage to the second voltage of 0.5:1.0 to 0.9:1.0 is achieved by a device having a 400 nm insulating film established between the first pixel electrode and the second pixel electrode. The specification discloses at page 31, lines 3-8, that the 400 nm insulating film "corresponds to a 0.9:1.0 voltage ratio and it is preferable that the above mentioned voltage ratio be greater than this." Therefore the Final Office Action concludes that the claimed ratio would be obvious Kaneko shows a 400 nm insulating film between the first pixel electrode and the second pixel electrode.

Based on this rationale, the Final Office Action considers that Kaneko shows in Figure 42B a liquid crystal display device having a first pixel electrode 94 and a second pixel electrode 96 separated by a film 98. Further, the Final Office Action relies on Kaneko at column 17, lines 57-60, for disclosing that the film 98 has a thickness of 4,000Å, or 400 nm as required by the specification.

However, Appellants respectfully submit that Kaneko shows in Figure 42B that a thickness of the insulating layer 98, ***between*** the first pixel electrode 94 and the second pixel electrode 96 is less than 400 nm because the second pixel electrode 96 accounts for at least 50 nm (500Å), as specifically disclosed by Kaneko at column 17, lines 16-19. Therefore, the thickness of the film 98 ***between*** the first pixel electrode 94 and the second pixel electrode 96 is 350 nm and not 400 nm as asserted by the Final Office Action. Thus, if the insulating layer in Kaneko is 350 nm, Appellants respectfully submit that Kaneko does not teach or suggest the claimed voltage ratio.

Appellants note that the specification specifically states at page 30, lines 8-10, "the insulating film established ***between*** the first layer of pixel electrode and second layer of pixel electrode is about 400 nm" (emphasis added). Appellants respectfully submit that the Final Office Action fails to consider the thickness of the film 98 in Kaneko ***between*** the first and second pixel electrodes.

In addition, Appellants respectfully submit that a voltage ratio of first and second pixel electrodes capacitively coupled as shown in Figure 1A of Michibayashi depends not only on the insulator thickness but also on the amount of overlap of the first and second pixel electrodes. Thus, the voltage ratio in Michibayashi is determined not only by the thickness of the insulator between the first and second pixel electrodes but also by the amount of overlap of the pixel electrodes. However, the Final Office Action did not establish that the applied art discloses the necessary amount of overlap for achieving the claimed voltage ratio.

Regarding the thickness of the insulating film, the Advisory Action adopts a different position than the Final Office Action by considering that not only the film 98 contributes to the thickness of the insulating film but also a 3,000Å thick amorphous silicon film 99 formed at the same level as the first pixel electrode 94 in Figure 42B of Michibayashi contributes to

the thickness of the insulating film. However, it is respectfully submitted that the silicon film 99 in Figure 42B of Michibayashi is not ***between*** the first and second pixel electrodes.

Therefore, Appellants respectfully submit that Figure 42B of Kaneko shows that the thickness of the film between the first pixel electrode 94 and the second pixel electrode 96 is 350 nm and not the at least 400 nm required by the specification in the paragraph bridging pages 30 and 31.

Thus, Appellants respectfully submit that one of ordinary skill in the art, when combining the teachings of Michibayashi and Kaneko, would not achieve a 400 nm insulating film between a first pixel electrode and a second pixel electrode because neither of Michibayashi and Kaneko shows such a feature.

Assuming arguendo that the applied art teaches forming a 400 nm insulating film between the pixel electrodes, because the applied art is silent about the amount of overlap of the pixel electrodes, it is respectfully submitted that one of ordinary skill in the art would not achieve the claimed voltage ratio based only on the 400 nm thickness of the insulating film. The one of ordinary skill in the art would need to know also the necessary amount of overlap of the pixel electrodes in Michibayashi for achieving the claimed voltage ratio.

In addition, Appellants respectfully submit that the disparate reference teachings of Michibayashi and Kaneko further raise the question of why the artisan would even consider these references for combination, a question the PTO must answer. See In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002), requiring the PTO to "explain the reasons one of ordinary skill in the art would have been motivated to select the references ...."

In effect, the Final Office Action does little more than attempt to show that parts of the inventive combination of Claim 1 were individually known in other arts and to suggest that such a showing is all that is necessary to establish a valid case of *prima face* obviousness.

The PTO reviewing court recently reviewed such a rationale and dismissed it in *In re Rouffet*, 149 F. 3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) as follows:

> As this court has stated, "virtually all [inventions] are combinations of old elements." *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 698, 218 USPQ 865, 870 (Fed. Cir. 1983); see also *Richdel, Inc. v. Sunspool Corp.*, 714 F.2d 1573, 1579-80, 219 USPQ 8, 12 (Fed. Cir. 1983) ("Most, if not all, inventions are combinations and mostly of old elements."). Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be "an illogical and inappropriate process by which to determine patentability." *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570, 38 USPQ2d 1551, 1554 (Fed. Cir. 1996). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. [emphasis added.]

There has been no such showing of those required reasons made in the final rejection.

Further, Appellants respectfully submit that independent Claims 9, 16, and 17 recite the same ratio of first and second voltages discussed above with regard to independent Claim 1. Accordingly, it is respectfully submitted that independent Claims 1, 9, 16, and 17 and each of the claims depending therefrom patentably distinguish over Michibayashi and Kaneko, either alone or in any proper combination.

Because the combination of Michibayashi and Kaneko is improper for the reasons discussed above and because the combination does not render obvious the claimed features, Appellants respectfully request the rejection of Claims 1, 9, 11, 12, 16, and 17 based on the combination of Michibayashi and Kaneko be reversed.

B. The combination of Michibayashi, Kaneko, and Kim does not teach or suggest each of the features of Claims 2 and 3.

Claims 2 and 3 depend from independent Claim 1, which has been discussed above. Kim does not teach or suggest an insulating film having a thickness of about 400 nm between first and second pixel electrodes. Because (i) the combination of Michibayashi and Kaneko does not render obvious the subject matter of Claim 1 as discussed in the previous subsection, and (ii) the teachings of Kim do not cure the deficiencies of (i), Appellants respectfully submit that the rejection of Claims 2 and 3 should be reversed for the same reasons.

C. The combination of Michibayashi, Kaneko, and Lee does not teach or suggest each of the features of Claim 8.

Claim 8 depends from independent Claim 1, which has been discussed above. Lee does not teach or suggest an insulating film having a thickness of about 400 nm between first and second pixel electrodes. Because (i) the combination of Michibayashi and Kaneko does not render obvious the subject matter of independent Claim 1, as discussed in subsection A, and (ii) the teachings of Lee do not cure the deficiencies of (i), Appellants respectfully submit that the rejection of Claim 8 should be reversed for the same reason.

CONCLUSION

As the Examiner has failed to establish any reasonable motivation to combine the references and even if they could, for some unknown reason, be combined, the reference teachings would fail to suggest all the limitations of the rejected claims, reversal of all outstanding rejections is respectfully requested.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1: A liquid crystal display device comprising:

transistors disposed at the intersections of gate lines and source lines;

pixel electrodes connected with the transistors;

opposite electrodes opposite to these pixel electrodes; and

liquid crystal held between said opposite electrodes and said pixel electrodes,

wherein said pixel electrodes comprise a first pixel electrode and a second pixel electrode disposed in a layer above an insulating film which is itself disposed in a layer above the first pixel electrode, and having a region that does not overlap with the first pixel electrode, and

wherein the first pixel electrode and second pixel electrode are electrically connected, the first pixel electrode applying a first electric field to the liquid crystal, and the second pixel electrode applying a second electric field whose strength is different from the first electric field to the liquid crystal, and

wherein a ratio of a first voltage applied to the liquid crystal by the first pixel electrode and a second voltage applied to the liquid crystal by the second pixel electrode is 0.5:1.0 to 0.9:1.0.

2: The liquid crystal display device, according to Claim 1, wherein the cumulative capacitance for stabilizing the pixel potential during the holding period is formed between said second pixel electrode and a storage capacitance electrode line or between the second pixel electrode and the preceding gate line adjacent thereto.

3: The liquid crystal display device, according to Claim 1, wherein said first pixel electrode is disposed in the same layer as the gate line.

4: The liquid crystal display device, according to Claim 1, wherein an insulating film is disposed in the layer below said gate line, and said first pixel electrode is disposed in the layer below said insulating film.

5: The active matrix liquid crystal display device, according to Claim 1,

wherein a first gate insulating film is disposed in the layer above said gate line, said first pixel electrode is disposed in the layer above the first gate insulating film, a second gate insulating film is disposed in the layer above the first pixel electrode, an interlayer insulating film is disposed in the layer above the second gate insulating film, and said second pixel electrode is disposed in the layer above the interlayer insulating film.

6: The liquid crystal display device, according to Claim 1, wherein said first pixel electrode is disposed in the same layer as the drain lines of said transistors.

7: The liquid crystal display device, according to Claim 6, wherein said first pixel electrode is directly connected to the drain electrode of said transistors.

8: The liquid crystal display device, according to Claim 1, wherein said second pixel electrode comprises an opening in the central portion of said second pixel electrode, and said insulating film and said liquid crystal are held between said first pixel electrode and opposite electrode in that opening.

9: A liquid crystal display device comprising:

transistors disposed at the intersections of gate lines and source lines;

pixel electrodes connected with the drain electrodes of the transistors;

opposite electrodes opposite to these pixel electrodes; and

liquid crystal held between said opposite electrodes and said pixel electrodes,

wherein said pixel electrodes comprise a first pixel electrode and a second pixel electrode disposed in a layer above an insulating layer which is itself disposed in a layer above the first pixel electrode, and having a region that does not overlap with the first pixel electrode, and

wherein the first pixel electrode and second pixel electrode are electrically connected with said drain electrode, the first pixel electrode applying first electric field to the liquid crystal, and the second pixel electrode applying a second electric field whose strength is different from the first electric field to the liquid crystal, and

wherein a ratio of a first voltage applied to the liquid crystal by the first pixel electrode and a second voltage applied to the liquid crystal by the second pixel electrode is 0.5:1.0 to 0.9:1.0.

10: (Cancelled)

11: The liquid crystal display device, according to Claim 1 or 9, wherein the thickness of said insulating layer is 500 nm or greater.

12: The liquid crystal display device, according to Claim 1 or 9, wherein said pixel electrode is a transparent electrode.

13: (Cancelled)

14: A liquid crystal display device, having liquid crystal held between a pair of substrates and including a plurality of pixels each having switching device, said liquid crystal display device further comprising:

means for applying spatially different voltages to the liquid crystal in one of the plurality of pixels;

an alignment layer disposed on the surface of each substrate in contact with the liquid crystal, for orienting said liquid crystal;

a polarizing plate disposed on the surface opposite to the surface of each of said substrates in contact with the liquid crystal; and

an optical compensating film disposed between said polarizing plate and said substrate having stabilized the orientation state of disco tic liquid crystal.

15: The liquid crystal display device, according to Claim 14, wherein the product of the birefringence Δn of said liquid crystal and the thickness d of the liquid crystal layer satisfies the relationship of $0.30\ \mu m \leq \Delta n \leq d \leq 0.50\ \mu m$.

16: A method for manufacturing a liquid crystal display device having transistors disposed at the intersections of gate lines and source lines, pixel electrodes connected with the transistors, opposite electrodes opposite to these pixel electrodes, and liquid crystal held between said opposite electrodes and said pixel electrodes, wherein said method comprises:

a step for manufacturing a first pixel electrode applying a first electric field to the liquid crystal;

a step for manufacturing an insulating layer in a layer above the first pixel electrode;

a step for manufacturing a second pixel electrode in a layer further above the insulating layer, said second pixel electrode having a region that does not overlap the first pixel electrode, and being electrically connected with the first pixel electrode and applying a second electric field whose strength is different from the first electric field to the liquid crystal, wherein a ratio of the voltages

applied to said liquid crystal by said first pixel electrode and said second pixel electrode is 0.5:1.0 to 0.9:1.0.

17: A method for manufacturing a liquid crystal display device having transistors disposed at the intersections of gate lines and source lines, pixel electrodes connected with the drain electrodes of the transistors, opposite electrodes opposite to these pixel electrodes, and liquid crystal held between said opposite electrodes and said pixel electrodes, wherein said method comprises:

a step for manufacturing a first pixel electrode electrically connected with said drain electrode and applying a first electric field to the liquid crystal;

a step for manufacturing an insulating layer in a layer above the first pixel electrode; and

a step for manufacturing a second pixel electrode in a layer further above the insulating layer, said second pixel electrode having a region that does not overlap the first pixel electrode, and being electrically connected with said drain electrode and applying a second electric field whose strength is different from the first electric field applied to the liquid crystal, wherein a ratio of the voltages applied to said liquid crystal by said first pixel electrode and said second pixel electrode is 0.5:1.0 to 0.9:1.0.

18: The liquid crystal display device according to Claim 1, wherein the cumulative capacitance for stabilizing the pixel potential during the holding period is formed between said second pixel electrode and a storage capacitance electrode line, and between the second pixel electrode and the preceding gate line adjacent thereto.

IX. EVIDENCE APPENDIX

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE